[Very bad OCR of the TANEX manual... I will type it like I did for the User Manual and the Basic Manual, ...when I find time]

Chapter 1

The data bus on the microtan 65 is directly connected to the 6502 microprocessor. In order to drive a complete system, it is necessary to buffer this bus, but to have done this on the microtan 65 would. have increased the cost of production, apart from the more obvious problem of insufficient space on the printed circuit board. Data bus buffers are therefore placed on TANEX, as they are only a necessity when microtan is expanded into a system, and this results in the system shown in the block diagram below.

The data bus buffers are controlled by the memory mapping logic on TANEX as follows.
When the 6502 microprocessor addresses memory located on the microtan 65 card, the buffers are disabled. Conversely, when memory which is external to the microtan 65 card is addressed, the buffers are enabled and the direction of data flow is determined by the state of the R/W line.

The only restriction imposed by this method of bus buffering is that a device capable of Direct Memory Access (DMA), such as TANDISC, cannot read or write directly to the RAM, ROM, or 1/0 ports on the microtan 65 card. Examined in more depth, this restriction is of little consequence, since a DMA device is unlikely to want to read the TAT\'BUG ROM, or to access any of the 1/0 ports on the microtan 65. In addition, this means that there is no way that a DMA device can accidentally overwrite TANBUG's system parameters, the processor stack, or the display memory, as these are located in the RAM on the microtan 65. The microtan system is therefore safe from system crashes which might otherwise be caused by a DMA transfer of data into this reserved memory area.

Chapter 2

Referring back to the microtan 65 manual, page 3-3, it is described there how microtan 65 operates with a very simple memory map of only three segments. When used in conjunction with TANEX, a more complex memory map is generated by the logic circuitry included on TANEX, which reconfigures the mapping as shown in the accompanying figure. In order to continue to use the RAM, ROM, and 1/0 on the microtan 65, three control lines are generated by TANEX; these are called RAME, ROME and IOE.
When. the microprocessor addresses memory between locations 0 and 3FF (i.e. the lowest IK of memory), the control line RAME is activated. By cutting the link LKRAM on the microtan 65, the IK RAM on microtan can then be enabled by RAME. When any other memory address is selected, RAME is inactive, and the microtan 65 RAM is disabled.

Addresses F800 to FFFF (the top 2K of memory) cause ROME to be active in a similar way, and by cutting link LKROM on the microtan 65, this signal allows the ROM on microtan (TANBUG) to be enabled. Although TANBUG is only in a 1K ROM, the system is not affected by allowing TANBUG to "roll-over" into the next but last 1K of memory space.

The third control line is IOE, which become active for addresses in the range BFFO to BFFF - the top 16 1/0 addresses. Again, cutting link LKIO on the microtan 65 allows this signal to enable microtan's 1/0 ports. Note that

IOE enables 16 1/0 addresses although microtan only uses 4 1/0 port addresses. Users should not use any of these 16 1/0 addresses for self constructed peripherals. As described in the microtan manual, user peripherals should use addresses starting at BCOO and work upwards.

Thus by cutting the three links LKRAM, LKROM and LKIO on the microtan 65, and connecting TANEX, full memory mappina of the microtan system is achieved. The RAM, ROM and 1/0 on TANEX itself are controlled by TANEX with no dependence on external signals. The addresses of each of these segments of TANEX are described in the appropriate section.
To aid' the decoding of 1/0 addresses, there is a control line on TANBUS called 1/0, which is bussed to all slots on the system motherboard. This signal is active (TTL high) when any 1/0 port is addressed, and therefore obviates the need for other peripheral devices to decode a full 16 bit address - only the lower order ten bits need to be decoded.

MEMORY ADDRESS FUNCTION

FFFF 1K ROM (TANBUG)

FCOO

FBFF (TANBUG REFLECTED -lK)

F800

F7FF

Fooo

EFFF 6K ROM

E800 TANEX

E7FF

Eooo

DFFF

Dooo 8K BASIC INTERPRETER

CFFF TANEX

cooo

BEEF BFFO - BFFF MICROTAN 65 I/O

IK I/O PORTS
BCOO

BBFF

40K RAM

TANRAM

2000

1FFF

7K RAM

TANEX

0400

03FF

0000 1K RAM ON MICROTAN 65

Fig 2-1 Full Memory Map of the Microtan System

Chapter 3

TANEX has provision for 7K of static RAM on board using the popular 2114 1K x 4 static RAM chip. The memory occupies addresses in the range 400 to 1FFF.

Only two 2114's (i.e. IK x 8) are supplied with TANEX in the minimum configuration, and these two chips should be inserted into locations N7 and N14 on the circuit board. Subsequent 2114's should be inserted in the ascending order indicated in Fig. 3.1, as this ensures that the available RAM is always in a contiguous block with the 1K of RAM located on the microtan 65. (No harm will be done by not following this recommendation if the user has particular need for non contiguous memory).

ADDRESS FUNCTION IC LOCATIONS
1FFF 1K TANEX
icoo RAM Nl N8
18FF IK TAMEX
1800 RAM N2 N9
17FF IK TANEX
1400 RAM N3 Nio
13FF 1K TANEX
1000 RAM N4 Nll
OFFF 1K TANEX
0800 RAM N5 N12
OAFF IK TANEX
0800 RAM N6 N13

07FF IK TANEX
0400 RAM N7 N14
03FF VDU DISPLAY

0200 MEMORY MICROTAN 65 RAM (lK)
OLFF MICROTAN 65 STACK OPERATES DOWN-
0040 USER RAM WARDS FROM OIFF
003F
0000 RESERVED FOR TANBUG

Fig 3-1 RAM Segment Memory Map

Chapter 4

TANEX can accept up to three 2K x 8 EPROMS and the two 4K x 8 ROMS that contain Microsoft BASIC. The BASIC interpreter (in
two 2332 ROMS) is located in the address space from COOO to DFFF,

and these two ROMS should be inserted into IC locations H2 and

j 2 . Each ROM must be placed in its correct socket for the BASIC
interpreter to operate, though no damage will ensue if they are accidentally transposed. Full information on this is included with the BASIC ROMS.

The three 2K byte EPROM positions accept the industry standard 2716 EPROM in its 5 volt only version. The IC locations and appropriate address range are shown in Fig. 4.1.

In order to make use of EPROM in the microtan system, the EPROM must be programmed with useful software. This could be the users own software, programmed into EPROM using an EPROM programmer, which itself may be either the microtan system programmer, or the users own. Alternatively, EPROMS containing proprietary software can be obtained from TANGERINE.

Interaction with TANBUG

The microtan system has been designed from the outset to be expandable, and TANBUG is no exception to this. Already powerful as a IK monitor, it contains within itself the necessary code to expand by a further 2K, when used in conjunction with TANEX.

Referring back to the microtan 65 manual, page 6-21, there is described TANBUG's error linking procedure. When TANBUG re-
ceives a command that is not in its repetoire, the program ex-
ecutes a jump to location F7F7, which is in the top EPROM on
TANEX. If no EPROM is installed, and the link LK1 is present,
location F7F7 is decoded as FFF7, and the program continues,
generating a '?' on the VDU. If the link LK1 is broken, address F7F7 is correctly decoded, and TANBUG's action will then depend upon the content of the EPROM in board location G2. If the user
wishes to use an EPROM in this socket, but without expanding TANBUG, then locations F7F7, F7F8 and F7F9 must be programmed with the instruction:

JMP FFF7

This will return TANBUG to the correct point. If the user does wish to expand TANBUG, then location F7F7 should have the instruction

JMP USERBUG

where 'USERBUG' is the start address of the users expansion software that will action any new commands. At the end of the users expansion software, a normal return to TANBUG should be executed using the instruction:

RTS

This will generate a carriage return/linefeed and re-enter TANBUG. Alternatively, the user expansion software can end with the following instructions:

PLA
PLA
JMP FC37

This will return directly to TANBUG with no change to the display. If, however, an error situation is the result, for example, because of an illegal command, the program should execute the instruction:

JMP FC89

This will print a question mark and carriage return and restart TANBUG appropriately.

The methods given above all presume that the users software has left the stack pointer in the same position as it was when the entry was made via address F7F7 i.e. that there are an equal number of JSR and RTS instructions in every flow path of the users
expansion software.

Note that TANGERINE Computer Sy@tems reserve the right to use this top EPROM location for the expanded system monitor, 'XBUG'.

ADDRESS FUNCTION IC LOCATIONS

FFFF

1K TANBUG ON MICROTAN 65

FCOO

FBFF

-lK REPEATED TANBUG RESERVED FOR EXPANSION

F800

F7FF
TANEX G2
2K E.PROM RESERVED FOR IIXBUG"

FOOO

EFFF

2K EPROM TANEX E2

E800

E7FF

2K EPROM TANEX D3

EOOO

DFFF

8K BASIC TANEX

INTERPRETER H2 and J2

cooo

Fig 4.1 ROM Segment Memory Map

Chapter 8

Although this chapter is intended for those who have purchased TANEX in kit form, it is recommended that purchasers of ready assembled TANEX also read through this, and the next section. Before beginning to assemble TANEX, please read right through the instructions carefully so that you understand all the operations involved.

Preparing your working surface

For assembling TANEX you will require a miniature soldering iron, thin multicored solder, pliers and wirecutters (both of the small variety).

As in the microtan 65, many of the integrated circuits are of the MOS type and can be damaged by static electricity, and we recommend you take the following precautions. Do not wear nylon clothes; ensure that your soldering iron is properly earthed; spread a sheet of aliminium foil (cooking foil) over your working area and earth it to a radiator or water pipe with a piece of wire.

Unpacking and identifying the parts

Unpack the kit and identify all the parts as listed below:
IC Sockets
2 off -8 pins
11 off -14 pins
6 off -16 pins
14 off -18 pins

5 off -24 pins
1 off -28 pins
2 off -40 pins

Integrated Circuits - minimum configuration TANEX

Ml 74LS30 K2 74LSOO
Li 74LS21 M3 74LS367
Kl 74LS138 L3 74LS32
jl 74LS138 M4 74LS367
Hl 74LS04 A3 LM358

'%-i 1 74LS139 N7 2114 (MOS)
M2 74LS367 N14 2114 (MOS)
L2 74LS74 A2 6522 (MOS)

In addition there will be 3 off 74LS367's which are to be fitted to the microtan 65 in IC locations Ml, M2 and M3.

Optional Integrated Circuits

C2 6522 additional VIA integrated circuit. (MOS'I
Fl 6551 serial IL/O option. (MOS)
D2 75150 serial 1/0 option.

N2 - N6, N8 - N13 additional RAM (see Fig. 3-1). (MOS)
Resistors (see microtan 65 manual page 2-4 for identification method)
RI IOK (brown, black orange) R10 2K2 (red, red, red)
R2 22K (red, red, orange) Rll 22OR (red, red, brown)
R3 22K (red, red, orange) R12 IOK (brown, black, orange)

R4 IK (brown, black, red) R 13 1 K (brown, black, red)
R5 120K (brown red, yellow) R14 22OR (red, red, brown)
R6 1 K (brown, black, red) R15 1 K (brown, black, red)
R7 120K (brown, red, yellow) R16 2K2 (red, red, red)
R8 22K (red, red, orange) R17 10K (brown, black, orange)
R9 2K2 (red, red, red) R18 1 K (brown, black, red)
R19 10K (brown, black, orange)

Capacitors

c 1 100n C2 100n

C3 - C23 decoupling capacitors (47n).

A-
Transistors
Trl - Tr3 BC184
Crystal
1. 8432M. Hz serial 1/0 option.
Connectors

64 pin Eurocard style edge connector.
4 way screw terminal block.
ASSE@@IBLING TANEX

a) Fit and solder the IC sockets, ensuring that they are the correct way round i.e. that the pin 1 identifier on the socket is at the same end as the identifier mark on the printed circuit board.

b) Fit and solder the resistors into their positions.

c) Fit and solder the capacitors into their positions.

d) Fit and solder the transistors into their positions.

e) Fit and solder links LKI and LK2 using the excess wire cut off from one of the resistors.

f) Fit and solder the screw terminal for the cassette interface, and the edge connector.

g) If you have purchased the serial 1/0 odtion, fit the crystal using the "sticky pad" provided and solder in place.

h) Insert the integrated circuits, ensuring that they are the correct way round, into their respective sockets, leaving the iViOS devices until last.

Assembly is now comdlete, but carefully double check to ensure that there are no solder blobs or bridges anywhere.

Further Assembly Hints

1) The circuit board is of the plated through hole type. This makes it difficult to remove a component once it has been soldered in place, so please double check that you have the right component in the right place before soldering it.

2) Do not apply pressure to the printed circuit board when soldering, as this may cause the tracks to lift and break.

3) A good solder joint is made by 'wetting' the tip of the solderin- iron with solder, and then placing the tip of the iron against the leg of the component where it emerges from the circuit board, and then feeding a small amount of solder against the tip, allowing it to flow around the area of the joint.

4) Wash your hands. Dirt and grease on the circuit board will make soldering difficult and unreliable.

5) Components are inserted on the side of the board with the white printing, and soldered ONLY on the opposite side.

6) Most important of all: DO NOT HURRY.

CONNECTING TO MICROTAN 65

In order to allow microtan 65 and TANEX to operate together, the following procedure, which assumes that the user has purchased a motherboard, must be followed:

1) Turn off the power supplies, and disconnect the microtan 65.

2) On microtan 65, cut through the three links marked LKRAM, LKROM and LKIO.

3 Three additional 74LS367 integrated circuits are supplied

with T.I.NEX. These should be inserted into microtan 65 in locations Ml, lv!2 and M3.

Now plug the two boards into the mini-motherboard or system

motherboard. Note that the edge connectors of the two boards

are offset at different positions to prevent confusion. The

track side of the motherboard, or mini-motherboard indicates
the correct positions for the printed circuit boards.

Reconnect to your power supply, and begin to enjoy the full power of your expanded microtan system.